IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: William M. Richardson

Serial No.: To Be Assigned

Filed: Herewith

For: METHOD AND SYSTEM FOR COMPUTER NETWORK LINK WITH UNDEFINED TERMINATION CONDITION

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the application as follows prior to examination on the merits.

IN THE CLAIMS

Please cancel claims 1-16 of the application.

Please add claims 17-41 to the application as follows:

What is claimed is:

17. (New) A method for analyzing a network link in a computer network, comprising:

generating a predetermined signal on the network link;

detecting a response of the link to the predetermined signal;

analyzing the response for an influence of a termination of the link, in which the step of analyzing comprises:

applying a short circuit threshold to the response of the link,

applying an open circuit threshold to the response of the link, and

searching the response of the link for a matched terminator;

locating the termination of the link in response to the application of the short circuit threshold, open circuit threshold, and search for the matched terminator; and

determining a time delay between the generation of the predetermined signal and the located termination.

18. (New) The method described in Claim 17, wherein the step of searching for the response of the matched terminator comprises determining a change in the influence of skin effects on the response resulting from the predetermined signal reaching the terminator.

19. (New) The method described in Claim 17, wherein generating the predetermined signal comprises generating a current step function on the network link.

20. (New) The method described in Claim 17, wherein the step of searching for the response of the matched terminator comprises detecting an inflection point in induced voltage on the network link.

21. (New) The method described in Claim 17, further comprising calculating the length of the network link to the terminator in response to the time delay.

22. (New) The method described in Claim 17, wherein the step of analyzing further comprises low pass filtering the response of the link and then detecting an inflection point in filtered response of the network link.

23. (New) The method described in Claim 17, wherein the step of analyzing further comprises low pass filtering the response of the link and then applying the thresholds to the filtered response.

24. (New) The method described in Claim 17, wherein the detection of the response of the link to the predetermined signal occurs at a non-terminator location on the network link.

25. (New) The method described in Claim 17, wherein the generation of the predetermined signal on the network link occurs at a non-terminator location on the network link.

26. (New) The method described in Claim 17, wherein the detection of the response of the link to the predetermined signal occurs on an operational computer network.

27. (New) The method described in Claim 17, wherein the generation of the predetermined signal on the network link occurs on an operational computer network.

28. (New) A network termination analysis device for a digital data network, comprising:

a function generator that injects a predetermined signal onto cabling of the network;

a digitizer that digitally samples the network's response to the predetermined signal; and

a system processor that downloads data from the digitizer to analyze the network's response to the predetermined signal and identify a time between the generation of the predetermined signal and a change in the network's response due to a termination of the network, in which the analysis comprises applying a short circuit threshold to the response, applying an open circuit threshold to the response, and searching the response for a matched terminator.

29. (New) A device as described in Claim 28, wherein the function generator injects a step function.

30. (New) The device described in Claim 28, wherein the system processor calculates at least one length of the cabling based on the time between the generation of the predetermined signal and a change in the network's response exceeding any one of the short or open circuit thresholds or the detection of the matched terminator.

31. (New) The device described in Claim 30, further comprising a monitor for displaying at least one calculated length of the cabling.

32. (New) The device described in Claim 31, wherein the display further indicates a maximum protocol-determined length for the cabling.

33. (New) The device described in Claim 28, wherein the function generator injects the predetermined signal onto cabling of the network at a non-terminator location.

34. (New) The device described in Claim 28, wherein the digitizer samples the network's response to the predetermined signal at a non-terminator location on the cabling.

35. (New) The device described in Claim 28, wherein the function generator injects the predetermined signal onto cabling of an operational network.

36. (New) The device described in Claim 28, wherein the digitizer samples the response to the predetermined signal of an operational network.

37. (New) A method for analyzing a network link in a computer network, comprising:

generating a predetermined signal on the network link;

detecting a response of the link to the predetermined signal;

filtering the response of the link by removing a contribution of a real component of the resistance of the link; and

displaying the filtered data to assist in the identification of impedance problems on the link.

38. (New) The method described in Claim 37, wherein the detection of the response of the link to the predetermined signal occurs at a non-terminator location on the network link.

39. (New) The method described in Claim 37, wherein the generation of the predetermined signal on the network link occurs at a non-terminator location on the network link.

40. (New) The method described in Claim 37, wherein the detection of the response of the link to the predetermined signal occurs on an operational computer network.

41. (New) The method described in Claim 37, wherein the generation of the predetermined signal on the network link occurs on an operational computer network.

IN THE SPECIFICATION:

Please delete the first full paragraph on page 1 and replace it with the paragraph set forth immediately below in clean form:

This application is a Continuation of U.S. Application No. 09/401,674, filed September 22, 1999, and claims priority to U.S. Application No. 08/890,486, filed July 9, 1997, now issued U.S. Patent No. 6,016,464 and U.S. Provisional Application Nos. 60/021,487, filed July 10, 1996, and 60/029,046, filed October 29, 1996, the entire teachings of these applications being incorporated herein by this reference.

Please delete the first full paragraph on page 4 and replace it with the paragraph set forth immediately below in clean form:

In general, according to one aspect, the invention is directed to a method for analyzing a network link on a computer network.

Specifically, it analyzes the link under any one of three criteria. Specifically, a short circuit threshold is applied to the link's response, an open circuit threshold is applied to the response, and a search is performed for a matched termination. A decision is then made based upon the application of these thresholds and the matched terminator search. Then, once the type of termination is found, a determination of the time delay between the generation of the predetermined signal and the located termination is performed.

Please delete the last paragraph beginning on page 6 and ending at the top of page 7 and replace it with the paragraph set forth immediately below in clean form:

A media interface unit (MIU) 100, or attachment unit, connects a digitizer 120 and signal generation circuits 150 to the physical layer of the network's links 10- 15 between terminating hub 16 and nodes 16-21, which include terminators 28-33. The MIU includes the receiver units R that collectively provide a two-channel input to the digitizer 120 through a summing network 36. The summing network 36 enables individual links to be monitored, or combines the signals of multiple links, on a channel of the digitizer 120. For adequate analog resolution, the digitizer should have at least a 500 MM sampling frequency with eight bits of resolution per sample and a long memory capacity of at least one megabyte of eight bit samples, or preferably 2 to 4 megabytes for 10 MBPS networks. Analysis of 100 MBPS to 1 GBPS networks is facilitated with correspondingly faster sampling frequencies and longer memory capacities.

Please also delete the first full paragraph on page 8 and replace it with the paragraph set forth immediately below in clean form:

Returning to Fig. 1A, the digitizer 120 comprises a buffering amplifier 122a, 122b on each of the two channels Ch1, Ch2. Two sample-and-hold circuits 124a, 124b downstream of each amplifier freeze the detected voltage in each channel for digitization by two analog-to-digital converters 126a, 126b. The digital outputs of the converters are written into two long memories 128a, 128b, one assigned to each channel Ch1, Ch2. The memories 128a, 128b

function as first-in, first-out (FIFO) buffers that continuously receive and store the output from the converters 126a, 126b until a trigger signal is received.

In accordance with 37 CFR 1.121(b)(iii), all paragraphs amended herein are set forth in a marked up version on the sheets attached to this amendment.

REMARKS

Applicant has canceled claims 1-16 and added new claims 17- 41 to the application. Applicant respectfully requests examination of these new claims. Applicant's amendments to the specification correct typographical errors or further describe aspects of the figures originally filed with the Application. No new matter has been added.

Respectfully submitted,

Date: May 31, 2001 By: _____

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CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

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Wendy Balabon
Signature

Date: May 31, 2001

Wendy Balabon

MARKED UP VERSION

Page 1, First Full Paragraph:

This application is a Continuation of U.S. Application No. 09/401,674, filed September 22, 1999, and claims priority to U.S. Application No. 08/890,486, filed July 9, 1997, now issued U.S. Patent No. 6,016,464 and ~~claims priority to~~ U.S. Provisional Application Nos. 60/021,487, filed July 10, 1996, and 60/029,046, filed October 29, 1996, the entire teachings of these applications being incorporated herein by this reference.

Page 4, First Full Paragraph:

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Page 6, Last Paragraph, Ending at Top of Page 7:

A media interface unit (MIU) 100, or attachment unit, connects a digitizer 120 and signal generation circuits 150 to the physical layer of the network's links 10-15 between terminating hub 16 and nodes 16-21, which include terminators 28-33. The MIU includes the receiver units R that collectively provide a two-channel input to the digitizer 120 through a summing network 36. The summing network 36 enables individual links to be monitored, or combines the signals of multiple links, on a channel of the digitizer 120. For adequate analog resolution, the digitizer should have at least a 500 MM sampling frequency with eight bits of resolution per sample and a long memory capacity of at least one megabyte of eight bit samples, or preferably 2 to 4 megabytes for 10 MBPS networks. Analysis of 100 MBPS to 1 GBPS networks is facilitated with correspondingly faster sampling frequencies and longer memory capacities.

Page 8, First Full Paragraph:

Returning to Fig. ~~1B~~ 1A, the digitizer 120 comprises a buffering amplifier 122a, 122b on each of the two channels Ch1, Ch2. Two sample-and-hold circuits 124a, 124b downstream of each amplifier freeze the detected voltage in each channel for digitization by two analog-to-digital converters 126a, 126b. The digital outputs of the converters are written into two long memories 128a, 128b, one assigned to each channel Ch1, Ch2. The memories 128a, 128b function as first-in, first-out (FIFO) buffers that continuously receive and store the output from the converters 126a, 126b until a trigger signal is received.